A DUAL-PORT SRAM IN A PROGRAMMABLE LOGIC DEVICE

ABSTRACT OF THE DISCLOSURE

Methods and apparatus for a dual-port SRAM in a programmable logic device. One embodiment provides a programmable logic integrated circuit including a dual-port memory. The memory includes a plurality of memory storage cells, and each memory storage cell has a memory cell having a first node and a second node, a first series of devices connected between a first data line and the first node of the memory cell, and a second series of devices connected between a second data line and the second node of the memory cell. A read cell is connected to the second node of the memory cell. A word line is connected to a first device in the first series of devices, a second device in the second series of devices, and the read cell.